InP HBT Transimpedance Amplifier for 43 Gb/s Optical Link Applications

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Abstract — **Transimpedance amplifiers with the bandwidth in the 50 GHz range for applications in long haul optical networks are presented. Transimpedance value is in the 220 to 300 Ω range, integrated input noise current ≈ 7.5 – 8.5 μA (0 – 60 GHz) and the output amplitude is between 600 mV_{pp} and 900 mV_{pp} (single ended) – dependent on the version. Circuits are designed in an InP HBT technology and consume 200 to 300 mW with +3.3 V supply voltage.**

I. Introduction

The development of components for broadband data transmission has been one of the driving forces in the semiconductor industry. With the 10 Gb/s systems fairly well established in the market the next step is to switch to higher data rates in the 40 – 50 Gb/s range and possibly to 80 – 100 Gb/s (NRZ) in the near future [1]. This paper presents the design of the input component of the optical link receiver: the transimpedance amplifier (TIA) for 43 Gb/s RZ or > 60 Gb/s NRZ transmission. Primary application of this TIA is in the long haul optical networks using optical amplifiers. Therefore relatively low electrical gain - 250 Ω - and high maximum input current from the photodiode – 4 mA – have been specified. Similar circuits in InP HEMT technology with 50 GHz bandwidth have recently been presented [2]. Several versions of the TIA have been designed, differentiated by the output drive capabilities, photodiode connection, and by the details in particular stages to optimize performance. The design is based the InP HBT technology developed by the Global Communication Semiconductors, Inc. (GCS) with transistor f_T and f_{max} exceeding 150 GHz.

II. Design Issues and Constraints

The structure of the chips (Fig. 1) follows typical arrangements. Input transimpedance stage defines noise properties of the chip and provides most of the gain. Single ended to differential converter accepts the full ITIA output signal swing and converts it to balanced outputs with good common mode rejection.

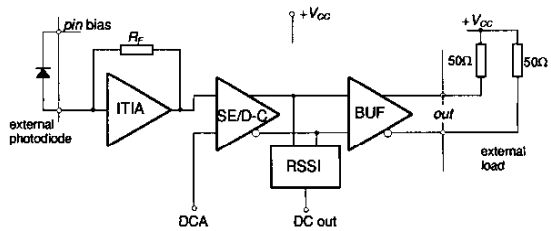

Fig. 1. Block diagram of the TIA chip. *ITIA* – input transimpedance stage, *SE/D-C* – single ended to differential signal converter, *RSSI* – received signal strength indicator, *BUF* – output buffer amplifier, *DCA* – output DC balance adjustment

Output buffer stage should supply enough current to the external 50 Ω loads to assure specified output amplitude – 600 mV_{pp} or 900 mV_{pp} in this case. This stage also provides moderate amount of signal limiting at maximum input current (3 to 4 mA).

Several factors restrict available optimization approaches to the design. The use of the indium phosphide HBT technology excludes *PNP* transistors, which would facilitate the use of dynamic loads in amplifier stages (high DC gain) and level shifting. High maximum input current value and the absence of dynamic loads cause large variations in the input transistor collector current and hence significant change of its properties vs. signal level. Analytic approach to circuit optimization is of limited value and experimental design based on nonlinear simulation must be used. Certain circuit parameters (feedback resistor R_F, bias currents) are determined by the overall specifications and little room is left for adjustments. The design is generally aimed at the best transient performance (eye diagram quality), which may conflict with the noise parameter improvement.

III. Input Stage Design

The solution used for the input stage is shown in Fig. 2. The circuit is intended for photodiodes with the anode output and positive diode bias voltage. Design

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was optimized for minimum noise within the limits imposed by the signal handling capability.

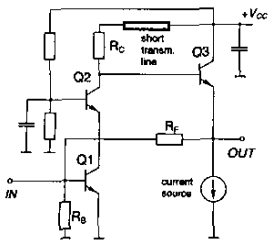

Fig. 2a. Input stage of the TIA

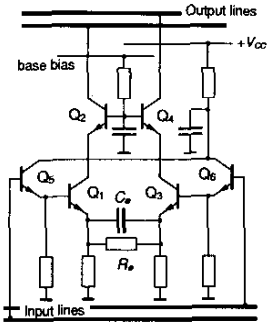

Fig. 2b. Elementary cell from the output stage

The TIA is built as a simple transimpedance stage with emitter follower (Q3) feedback [3]. Cascode input stage was used for increased bandwidth. Inductive compensation with short sections of narrow transmission lines is used in gain stages.

This TIA has been designed to connect to the external photodiode chip with bonding wires. The inductance of the bonding wire poses a real challenge in such a broadband design. It may be used to extend the bandwidth of the system but the circuit should not be very sensitive to the inevitable variations in the bonding wire length.

Simple model of the diode-TIA interface is shown in Fig. 3. The current transfer ratio $A_{it} = I_{in}/I_d$ for this model is given by (1).

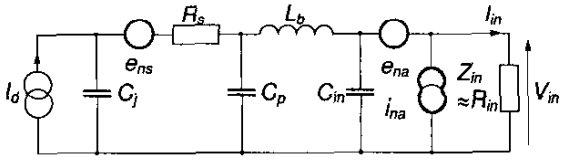

Fig. 3. Model of the TIA input circuit including photodiode and noise sources. C_j – diode junction capacitance, R_s – diode series resistance, C_p – contact pad capacitance, L_b bonding wire inductance, C_{in} – input TIA chip capacitance – mostly bonding pad, Z_{in} – input stage input impedance, e_{na}, I_{na} – amplifier noise sources (including R_B and R_F), e_{ns} – thermal noise of the diode resistance R_s

The generally low-pass function may have complex poles dependent on the value of L_b and Z_{in}. For the circuits presented here Z_{in} has relatively small imaginary part (<25% R_{in}) and R_{in} varies no more than 30% across full bandwidth. Subsequently it was assumed that $Z_{in} \approx R_{in} \approx \text{const}(f)$.

$$A_{it}(s) = \frac{I_{in}}{I_d} = \frac{1}{1 + as + bs^2 + cs^3 + ds^4} = \frac{1}{D}$$

where

$$\begin{aligned} a &= R_{in}(C_j + C_p + C_{in}) + R_s C_j \\ b &= L_b(C_j + C_p) + R_s C_j R_{in}(C_{in} + C_p) \\ c &= L_b\left[C_{in} R_{in}(C_p + C_j) + C_p C_j R_s\right] \\ d &= L_b C_p R_s C_j R_{in} C_{in} \end{aligned} \qquad (1)$$

Moderate gain peaking in the input stage is advantageous to compensate for the loss of gain in the following stages. Here it was arbitrarily assumed that 3 dB of gain increase at 50 GHz is a good solution. The required L_b in this case may be computed from (1). Fig. 4 shows the variation in gain at f = 50 GHz vs. L_b computed for the representative data: C_j = 30 fF, R_s = 20 Ω, C_p = 20 fF, C_{in} = 15 fF. Sensitivity to L_b variations may be evaluated from this figure as well.

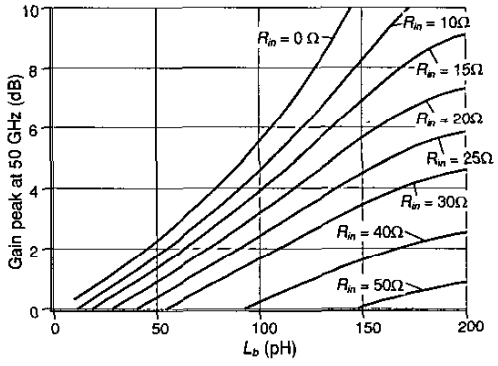

Fig. 4. Gain peaking at f = 50 GHz vs. L_{bw} for various input resistances R_{in}

It must be noted that usually L_b includes the contribution from two bondings to the diode chip and practical minimal value of L_b is on the order of 100 pH. Thus there is no reason to design the TIA for the lowest possible R_{in} if the bonding wire connection is planned. The upper limit of R_{in} is dictated by the resulting bandwidth. For the data used above that limit is ≈ 45 Ω under the condition that the peak frequency should not drop below 50 GHz.

The amount of peaking that may be used at the input is also limited by the allowable group delay variation. The group delay of the transfer function (1) is shown in Fig. 5. Large changes in τ_g occurring above 60 GHz are not very critical (10Ω and 20Ω case) but the peaks in the 30 – 60 GHz range tend to add to similar peaks from the stages following.

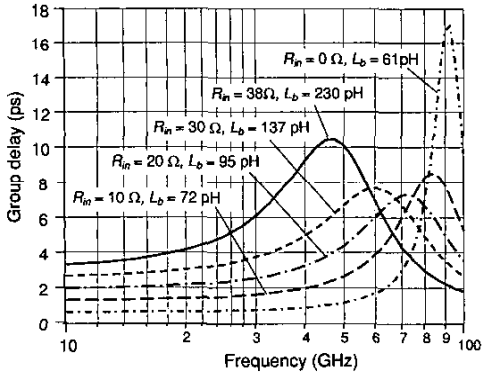

Fig. 5. Group delay vs. frequency - bonding wire inductance selected for 3 dB gain peaking at 50 GHz

Noise performance of the TIA is determined typically by transistors used and there are limited options for improvement with certain components fixed by other requirements. Input referred noise would be improved with L_b values larger that are needed for acceptable transient response.

$$\overline{I_{ni}^2} = \overline{e_{ns}^2} \cdot \frac{\omega^2 C_j^2}{|D|^2} \cdot + \overline{e_{na}^2} \cdot \left|\frac{A}{D}\right|^2 + \overline{i_{na}^2} \cdot \left|\frac{B}{D}\right|^2 +$$

$$+ 2 \cdot \mathrm{Re}(C_a \cdot \overline{A \cdot B^*} \cdot \sqrt{\overline{e_{na}^2} \cdot \overline{i_{na}^2}})$$

where

$$A(j\omega) = -\omega^2 R_s C_j (C_p + C_{in}) + \omega^4 R_s C_j C_p C_{in} L_b +$$

$$+ j\omega\left[C_j + C_p + C_{in} - \omega^2 L_b C_{in}(C_p + C_j)\right]$$

$$B(j\omega) = 1 - \omega^2 L_b (C_p + C_j) + j\omega R_s C_j (1 - \omega^2 L_b C_p)$$

$D(j\omega)$ - denominator of (1)

Noise current density referred to input is given by the equation above.

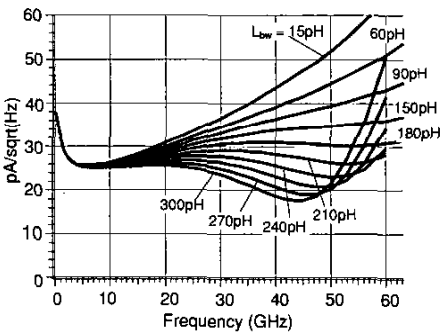

Fig. 6. Input noise current density vs. frequency for the circuit in Fig. 2a (simulation).

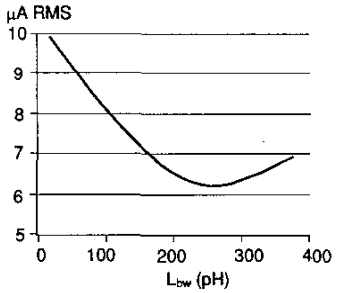

Fig. 7. Equivalent input noise current (I_d terminals). Integration bandwidth is 0.01 ÷ 60 GHz

Fig. 6.and 7 show noise performance of the circuit. Optimum L_{bw} value of 260 pH is unacceptable in this case because of too much jitter in the output eye diagram. Typically 140 pH bonding wire was used.

IV. Output Stage and General Design Approach

Output buffer contains a number of cells shown in Fig. 2b connected in parallel. This version contains three cells with 1x5 μm transistors. Cascode provides largest bandwidth with good linearity and high output impedance, which helps to maintain low reflections at the output ($|S_{22}|$ < -10 dB to >50 GHz). Moderate amount of gain compensation was used in the differential stage with C_e capacitor. Extremely broadband circuits like the TIAs presented here require very careful consideration of design details. Certain portions of chips were modeled with the electromagnetic simulator to account properly for discontinuities and transmission line properties. Based on these simulations the models have been created for the Cadence® software, which was used for design. Particular attention was paid to the bias distribution and decoupling network. to decrease ringing and group delay deviation.

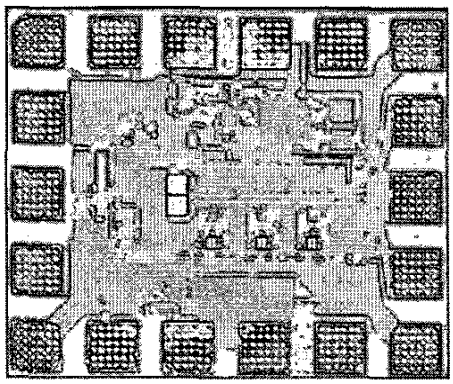

Fig. 8. Photograph of chip with the RSSI circuit

V. EXPERIMENTAL RESULTS

TIA circuits have been tested both on wafer and in packaged form as an optical receiver. The photodiode and the package were provided by u2t Photonics AG [4]. Selected test results are shown in Fig. 9 - 11.

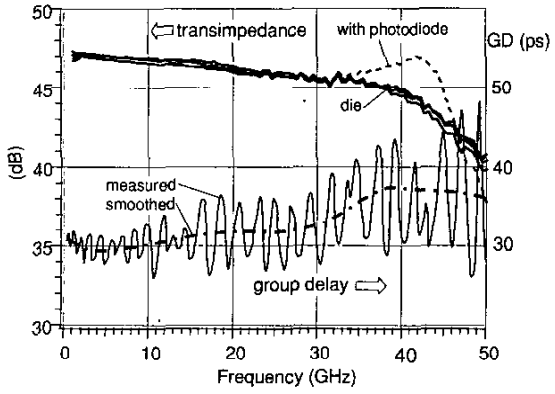

Fig. 9. Transimpedance and group delay computed from measured S parameters for the 'bare' die and for the photodiode with C_j = 30 fF and L_{bw} = 140 nH

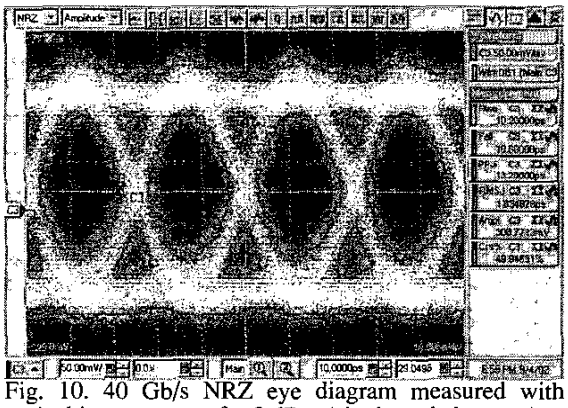

Fig. 10. 40 Gb/s NRZ eye diagram measured with optical input power of + 3 dBm (single ended output)

Typical bandwidth is about 42 GHz for trans-impedance ($Z_s = \infty$) and in the 45 – 48 GHz range with a photodiode and a bonding wire $L_{bw} \approx 120 - 150$ pH.

High ambient temperatures (85 - 100°C) degrade the bandwidth by about 10 – 12 %. Input current noise integrated over 60 GHz bandwidth is approx. 7.5 μA for L_{bw} = 150 pH.

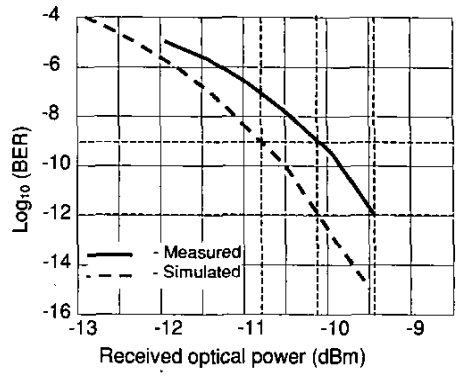

Fig. 11. Simulated and measured bit error rate (BER) for the optical module

V. CONCLUSIONS

Transimpdance amplifiers presented here achieve >45 GHz bandwidth with very flat group delay response (better than ± 5 ps), low input referred noise: < 7.5 μA RMS and good output matching . These circuits achieve –9.5 dBm optical sensitivity (for BER = 10^{-12}) and are well suited for optical receivers for fibre systems with 43 Gb/s RZ and > 60 Gb/s NZR modulation.

ACKNOWLEDGEMENT

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